PC755BM8
RISC Microprocessor Multichip Package

Datasheet - *Preliminary Specification*

Features

- **PC755BM8 RISC Miprocessor**
- **Dedicated 1-megabyte SSRAM L2 Cache, Configured as 128K x 72**
- **21 mm x 25 mm, 255 Ceramic Ball Grid Array (CBGA)**
- **Maximum Core Frequency = 350 MHz**
- **Maximum L2 Cache Frequency = 175 MHz**
- **Maximum 60x Bus Frequency = 66 MHz**

Description

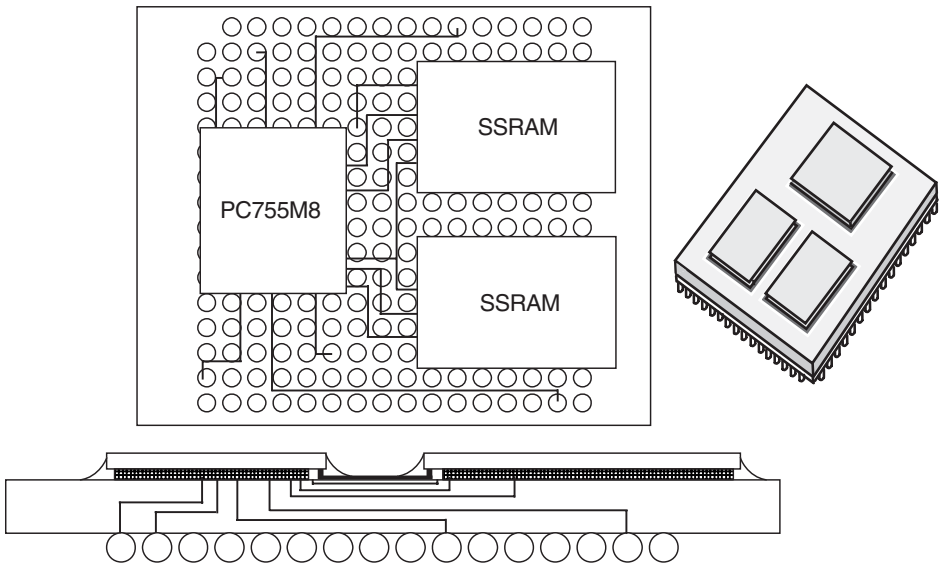
The PC755BM8 multichip package is targeted for high-performance, space-sensitive, low-power systems and supports the following power management features: doze, nap, sleep and dynamic power management.

The PC755BM8 is offered in industrial and military temperature ranges and is well suited for embedded applications.

Screening

This product is manufactured in full compliance with:

- **CBGA Up Screenings Based on e2v Standards**
- **Full Military Temperature Range (T_J = –55° C, +125° C)**
- **Industrial Temperature Range (T_J = –40° C, +110° C)**



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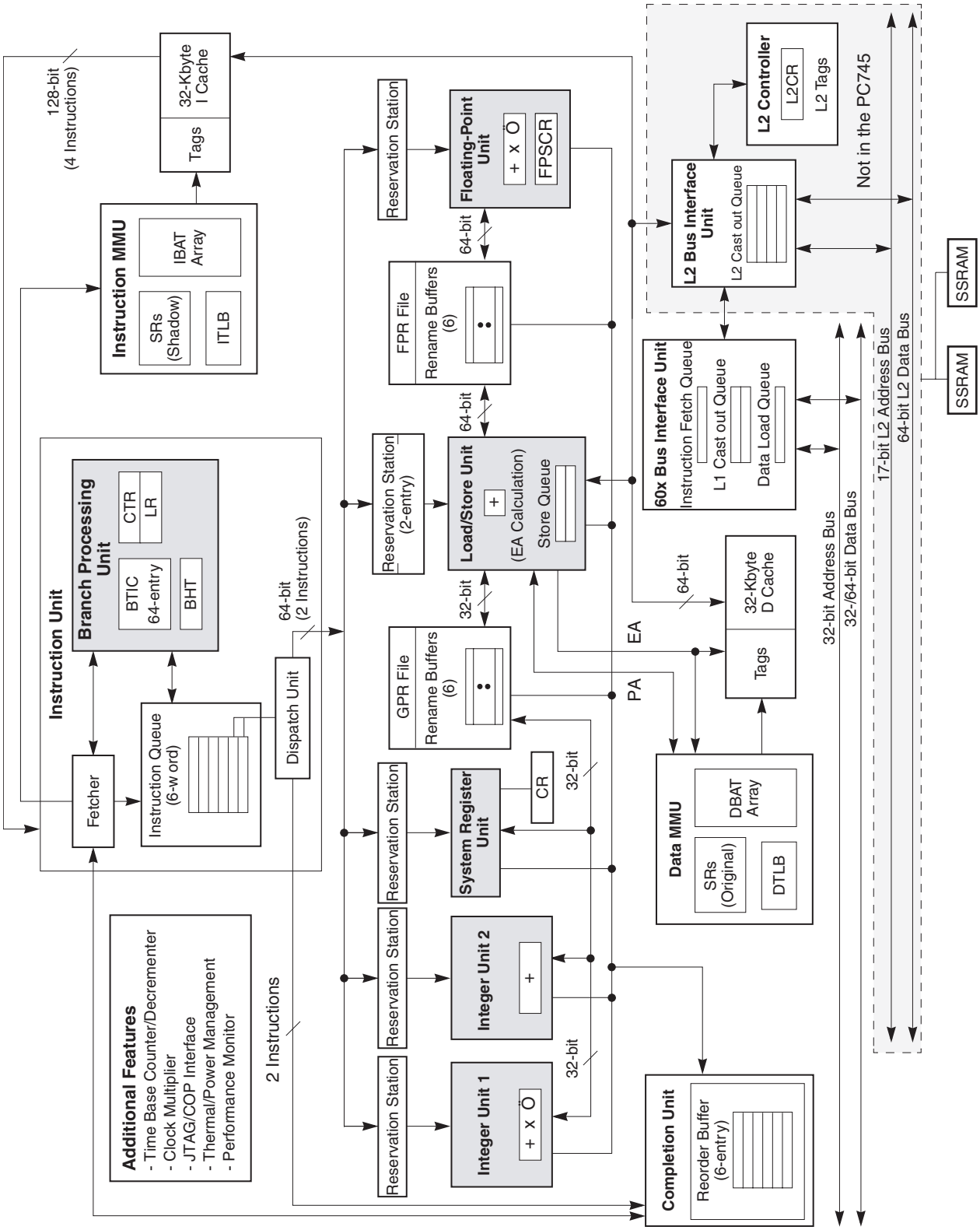
1. Block Diagram

Figure 1-1. PC755BM8 Microprocessor Block Diagram



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1.1 Major Features

This section summarizes features of the PC755BM8's implementation of the Power Architecture™. Major features of the PC755BM8 are as follows:

- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving 2 speculations)
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative Branch Target Instruction Cache (BTIC) for eliminating branch delay slots
- Dispatch Unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 6-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes
- Fixed Point Units (FXUs) that share 32 GPRs for Integer Operands
  - Fixed Point Unit 1 (FXU1) – multiply, divide, shift, rotate, arithmetic, logical
  - Fixed Point Unit 2 (FXU2) – shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point Unit and a 32-entry FPR File
  - Support for IEEE-754 standard single and double precision floating-point arithmetic
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Single-entry reservation station
  - Supports non-IEEE mode for time-critical operations
- System Unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions

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- Load/Store Unit
  - One cycle load or store cache access (byte, half-word, word, double-word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle unaligned access within double word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big and Little-endian byte addressing supported
  - Misaligned Little-endian supported
  - Level 1 Cache structure
  - 32K, 32 bytes line, 8-way set associative instruction cache (iL1)
  - 32K, 32 bytes line, 8-way set associative data cache (dL1)
  - Cache locking for both instruction and data caches, selectable by group of ways
  - Single-cycle cache access
  - Pseudo least-recently used (PLRU) replacement
  - Copy-back or Write through data cache (on a page by page basis)
  - Supports all Power Architecture memory coherency modes
  - Non-blocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Memory Management Unit
  - 128-entry, 2-way set associative instruction TLB
  - 128-entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - 8-instruction BATs and 8-data BATs
  - 8 SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus Interface
  - Compatible with 60X processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5V and 3.3V
  - Parity checking on both address and data buses

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- Power Management
  - Low-power design with thermal requirements – very similar to PC740/750
  - Selectable interface voltage of 1.8V/2.0V can reduce power in output buffers (compared to 3.3V)
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
- Integrated Thermal Management Assist Unit
  - On-chip thermal sensor and control logic
  - Thermal Management Interrupt for software regulation of junction temperature

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1.2 Signal Description

Figure 1-2. PC755BM8 Microprocessor Signal Groups

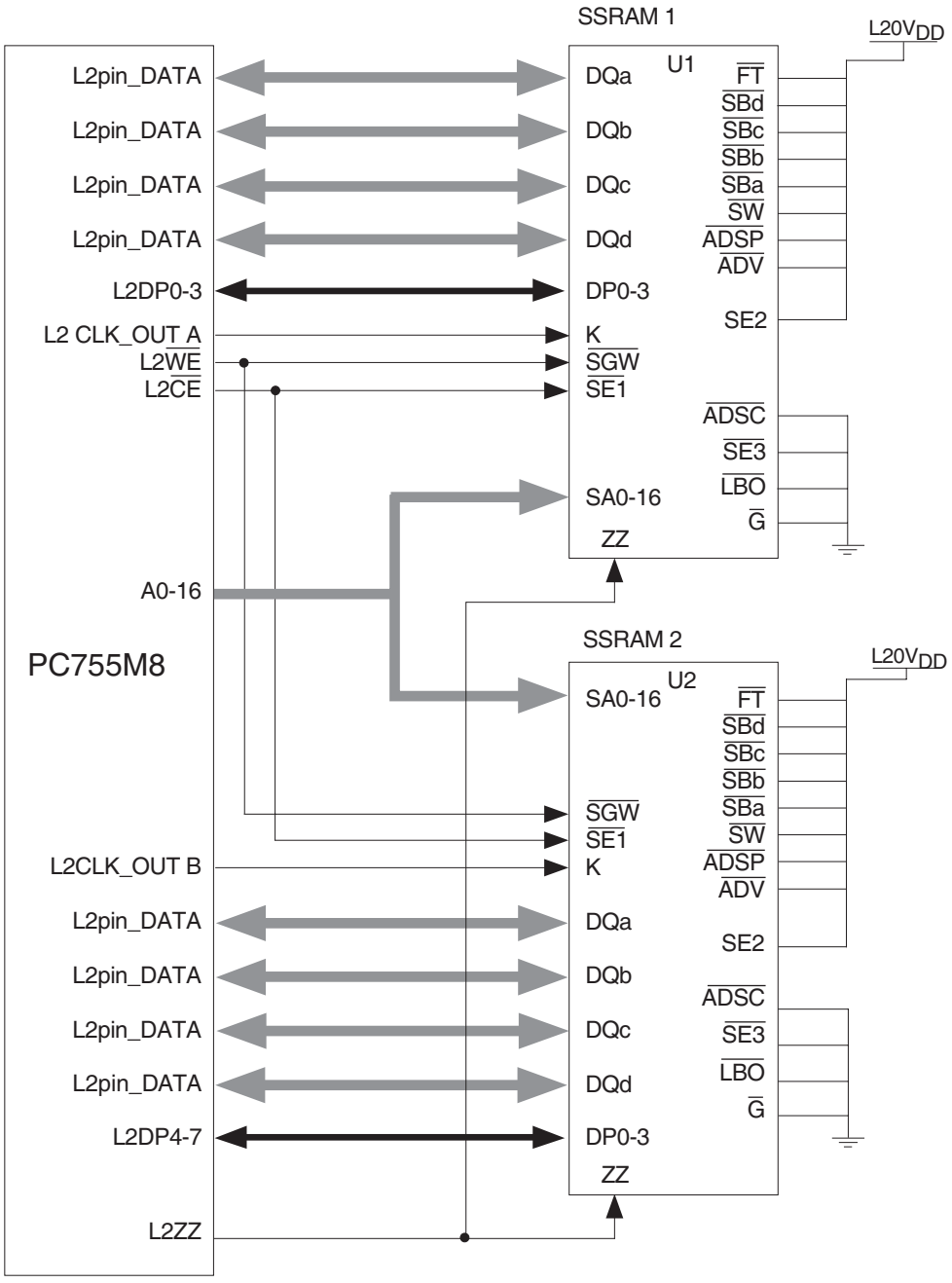

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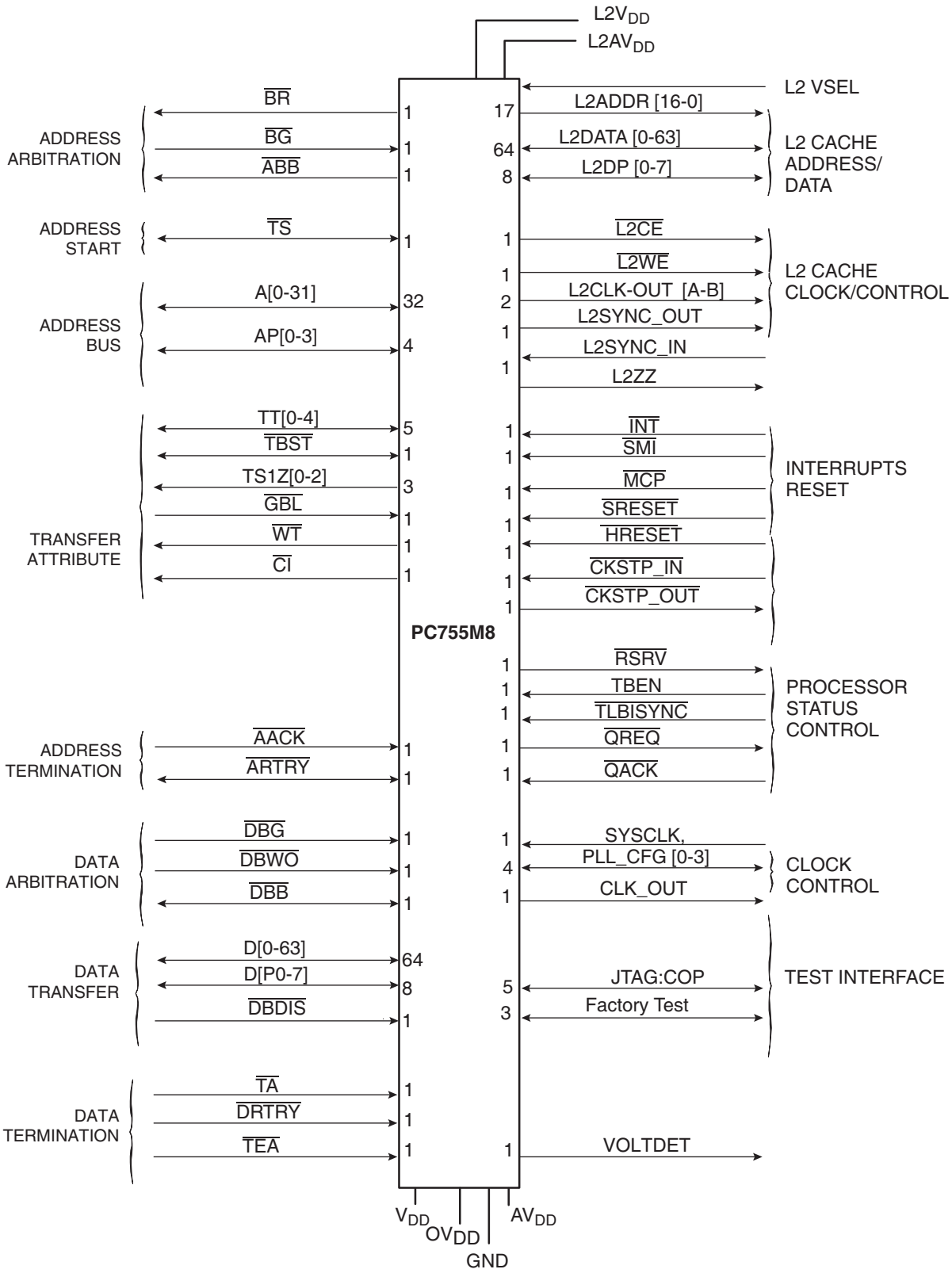
Figure 1-3. PC755BM8 Microprocessor Signal Groups (continued)



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2. Detailed Specification

2.1 Scope

This drawing describes the specific requirements for the PC755BM8 microprocessor, in compliance with e2v standard screening.

3. Applicable Documents

1. In accordance with MIL-STD-883: Test methods and procedures for electronics
2. In accordance with MIL-PRF-38535 appendix A: General specifications for microcircuits

3.1 Requirements

3.1.1 General

The microcircuits are in accordance with the applicable documents and as specified herein.

3.2 Design and Construction

3.2.1 Terminal Connections

Depending on the package, the terminal connections are shown in Table 5-1, Table 3-1 and Figure 1-2.

3.3 Absolute Maximum Rating

Table 3-1. Absolute Maximum Ratings(1)

Characteristic		Symbol	Maximum Value	Unit
Core supply voltage(4)		V_{DD}	–0.3 to 2.5	V
PLL supply voltage(4)		AV_{DD}	–0.3 to 2.5	V
L2 DLL supply voltage(4)		$L2AV_{DD}$	–0.3 to 2.5	V
Processor bus supply voltage(3)		OV_{DD}	–0.3 to 3.465	V
L2 bus supply voltage(3)		$L2OV_{DD}$	–0.3 to 3.465	V
Input voltage	Processor bus(2)(5)	V_{IN}	–0.3 to OV_{DD} + 0.3V	V
	L2 Bus(2)(5)	V_{IN}	–0.3 to $L2OV_{DD}$ + 0.3V	V
	JTAG Signals	V_{IN}	–0.3 to 3.6	V
Storage temperature range		T_{STG}	–65 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 3-2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3V at any time including during power-on reset.
3. Caution: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. Caution: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3-1.

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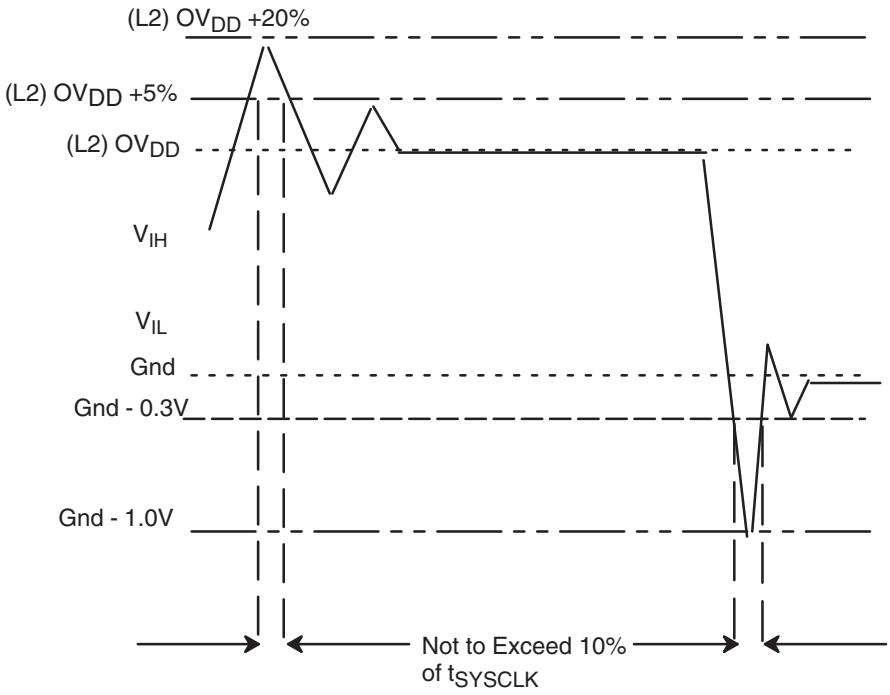
Figure 3-1. Overshoot/Undershoot Voltage



The PC755BM8 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC755BM8 core voltage must always be provided at nominal 2.0V (see Table 3-3 for actual recommended core voltage). Voltage to the L2 I/Os and Processor Interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 3-2. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 3-2. Input Threshold Voltage Setting[(1)(2)]

Part Revision	BVSEL Signal	L2VSEL Signal	Processor Bus nterface Voltage	L2 Bus Interface Voltage
E	0	0	Not Available	Not Available
	0	1	Not Available	2.5V/3.3V
	1	0	2.5V/3.3V	Not Available
	1	1	2.5V/3.3V	2.5V/3.3V

Notes: 1. The input threshold settings above are different for all revisions prior to Rev 2.8 (Rev E). For more information, contact your local e2v sales office.

2. Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.

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3.4 Recommended Operating Conditions

Table 3-3. Recommended Operating Conditions[1]

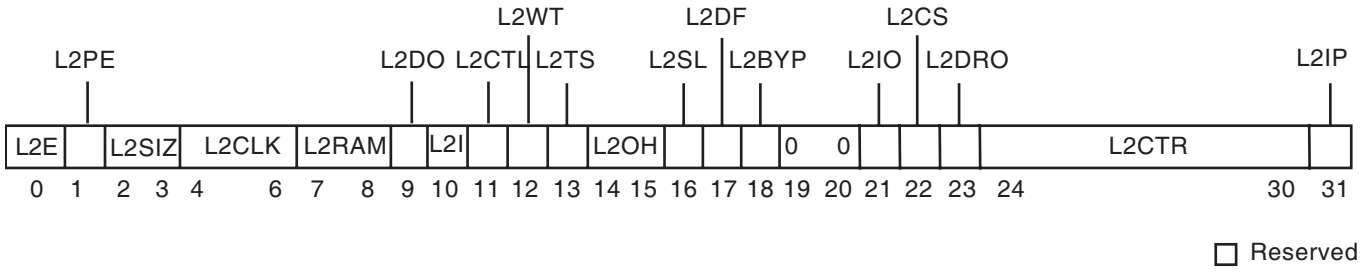
Characteristic		Symbol	Recommended Value 300 MHz, 350 MHz Min	Recommended Value 300 MHz, 350 MHz Max	Unit
Core supply voltage[3]		V_{DD}	1.9	2.10	V
PLL supply voltage[3]		AV_{DD}	1.9	2.10	V
L2 DLL supply voltage[3]		$L2AV_{DD}$	1.9	2.10	V
Processor bus supply voltage[2][4][5]	BVSEL = 1	OV_{DD}	2.375	2.625	V
			3.135	3.465	V
L2 bus supply voltage[2][4][5]	L2VSEL = 1	$L2OV_{DD}$	3.135	3.465	V
Input voltage	Processor bus	V_{IN}	GND	OV_{DD}	V
	L2 Bus	V_{IN}	GND	$L2OV_{DD}$	V
	JTAG Signals	V_{IN}	GND	OV_{DD}	V
Die-junction temperature	Military temperature range	T_j	–55	125	°C
	Industrial temperature	T_j	–40	110	°C

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support.
3. 2.0V nominal.
4. 2.5V nominal.
5. 3.3V nominal.

3.5 L2 Cache Control Register (L2CR)

The L2 cache control register, shown in Figure 3-2, is a supervisor-level, implementation-specific SPR used to configure and operate the L2 cache. It is cleared by hard reset or power-on reset.

Figure 3-2. L2 Cache Control Register (L2CR)



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The L2CR bits are described in Table 3-4.

Table 3-4. L2CR Bit Settings

Bit	Name	Function
0	L2E	L2 enable – Enables L2 cache operation (including snooping) starting with the next transaction the L2 cache unit receives. Before enabling the L2 cache, the L2 clock must be configured through L2CR[2CLK], and the L2 DLL must stabilize. All other L2CR bits must be set appropriately. The L2 cache may need to be invalidated globally.
1	L2PE	L2 data parity generation and checking enable – Enables parity generation and checking for the L2 data RAM interface. When disabled, generated parity is always zeros. L2 Parity is supported by PC755BM8, but is dependent on application.
2 – 3	L2SIZ	L2 size – Should be set according to the size of the L2 data RAMs used. 11 1-Mbyte – Setting for PC755BM8
4 – 6	L2CLK	L2 clock ratio (core-to-L2 frequency divider) – Specifies the clock divider ratio based at the core clock frequency that the L2 data RAM interface is to operate at. When these bits are cleared, the L2 clock is stopped and the on-chip DLL for the L2 interface is disabled. For nonzero values, the processor generates the L2 clock and the on-chip DLL is enabled. After the L2 clock ratio is chosen, the DLL must stabilize before the L2 interface can be enabled. The resulting L2 clock frequency cannot be slower than the clock frequency of the 60x bus interface. 000 L2 clock and DLL disabled 001 ÷ 1 010 ÷ 1.5 011 Reserved 100 ÷ 2 – Setting for PC755BM8 101 ÷ 2.5 110 ÷ 3 111 Reserved
7 - 8	L2RAM	L2 RAM type – Configures the L2 RAM interface for the type of synchronous SRAMs used: • Pipelined (register-register) synchronous burst SRAMs that clock addresses in and clock data out The PC755BM8 does not burst data into the L2 cache, it generates an address for each access. 10 Pipelined (register-register) synchronous burst SRAM – Setting for PC755BM8
9	L2DO	L2 data-only – Setting this bit enables data-only operation in the L2 cache. For this operation, instruction transactions from the L1 instruction cache already cached in the L2 cache can hit in the L2, but new instruction transactions from the L1 instruction cache are treated as cache-inhibited (bypass L2 cache, no L2 checking done). When both L2DO and L2IO are set, the L2 cache is effectively locked (cache misses do not cause new entries to be allocated but write hits use the L2).
10	L2I	L2 global invalidate – Setting L2I invalidates the L2 cache globally by clearing the L2 bits including status bits. This bit must not be set while the L2 cache is enabled. See Freescale® User's manual for L2 Invalidation procedure.
11	L2CTL	L2 RAM control (ZZ enable) – Setting L2CTL enables the automatic operation of the L2ZZ (low-power mode) signal for cache RAMs. Sleep mode is supported by the PC755BM8 – While L2CTL is asserted, L2ZZ asserts automatically when the device enters nap or sleep mode and negates automatically when the device exits nap or sleep mode. This bit should not be set when the device is in nap mode and snooping is to be performed through deassertion of $\overline{\text{QACK}}$.
12	L2WT	L2 write-through – Setting L2WT selects write-through mode (rather than the default write-back mode) so all writes to the L2 cache also write through to the 60x bus. For these writes, the L2 cache entry is always marked as exclusive rather than modified. This bit must never be asserted after the L2 cache has been enabled as previously-modified lines can get remarked as exclusive during normal operation.
13	L2TS	L2 test support – Setting L2TS causes cache block pushes from the L1 data cache that result from **dcbf** and **dcbst** instructions to be written only into the L2 cache and marked valid, rather than being written only to the 60x bus and marked invalid in the L2 cache in case of hit. This bit allows a **dcbz/dcbf** instruction sequence to be used with the L1 cache enabled to easily initialize the L2 cache with any address and data information. This bit also keeps **dcbz** instructions from being broadcast on the 60x and single-beat cacheable store misses in the L2 from being written to the 60x bus. **0: Setting for the L2 Test Support** as this bit is reserved for tests.
14 - 15	L2OH	L2 output hold – These bits configure output hold time for address, data, and control signals driven to the L2 data RAMs. 00 Least Hold Time - Setting for PC755BM8

Table 3-4. L2CR Bit Settings (Continued)

Bit	Name	Function
16	L2SL	L2 DLL slow – Setting L2SL increases the delay of each tap of the DLL delay line. It is intended to increase the delay through the DLL to accommodate slower L2 RAM bus frequencies. **0: Setting for PC755BM8** because L2 RAM interface is operated above 100 MHz.
17	L2DF	L2 differential clock – This mode supports the differential clock requirements of late-write SRAMs. **0: Setting for PC755BM8** because late-write SRAMs are not used.
18	L2BYP	L2 DLL bypass is reserved. 0: Setting for PC755BM8
19 – 20	–	Reserved – These bits are implemented but not used; keep at 0 for future compatibility.
21	L2IO	L2 instruction-only – Setting this bit enables instruction-only operation in the L2 cache. For this operation, data transactions from the L1 data cache already cached in the L2 cache can hit in the L2 (including writes), but new data transactions (transactions that miss in the L2) from the L1 data cache are treated as cache-inhibited (bypass L2 cache, no L2 checking done). When both L2DO and L2IO are set, the L2 cache is effectively locked (cache misses do not cause new entries to be allocated but write hits use the L2). Note that this bit can be programmed dynamically.
22	L2CS	L2 clock stop – Setting this bit causes the L2 clocks to the SRAMs to automatically stop whenever the MPC755 enters nap or sleep modes, and automatically restart when exiting those modes (including for snooping during nap mode). It operates by asynchronously gating off the L2CLK_OUT [A:B] signals while in nap or sleep mode. The L2SYNC_OUT/SYNC_IN path remains in operation, keeping the DLL synchronized. This bit is provided as a power-saving alternative to the L2CTL bit and its corresponding ZZ pin, which may not be useful for dynamic stopping/restarting of the L2 interface from nap and sleep modes due to the relatively long recovery time from ZZ negation that the SRAM requires.
23	L2DRO	L2 DLL rollover – Setting this bit enables a potential rollover (or actual rollover) condition of the DLL to cause a checkstop for the processor. A potential rollover condition occurs when the DLL is selecting the last tap of the delay line, and thus may risk rolling over to the first tap with one adjustment while in the process of keeping synchronized. Such a condition is improper operation for the DLL, and, while this condition is not expected, it allows detection for added security. This bit should be set when the DLL is first enabled (set with the L2CLK bits) to detect rollover during initial synchronization. It could also be set when the L2 cache is enabled (with L2E bit) after the DLL has achieved its initial lock.
24 - 30	L2CTR	L2 DLL counter (read-only) – These bits indicate the current value of the DLL counter (0 to 127). They are asynchronously read when the L2CR is read, and as such should be read at least twice with the same value in case the value is asynchronously caught in transition. These bits are intended to provide observability of where in the 128-bit delay chain the DLL is at any given time. Generally, the DLL operation should be considered at risk if it is found to be within a couple of taps of its beginning or end point (tap 0 or tap 128).
31	L2IP	L2 global invalidate in progress (read only) – See the Freescale user's manual for L2 Invalidation procedure.

3.6 Power consideration

3.6.1 Power management

The PC755BM8 provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are as follows:

- Full-power: This is the default power state of the PC755BM8. The PC755BM8 is fully powered and the internal functional units operate at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution, or external hardware.
- Doze: All the functional units of the PC755BM8 are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or machine check brings the PC755BM8 into the full-power state. The PC755BM8 in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.

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- Nap: The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The PC755BM8 returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or a machine check input (MCP). A return to full-power state from a nap state takes only a few processor clock cycles. When the processor is in nap mode, if $\overline{\text{QACK}}$ is negated, the processor is put in doze mode to support snooping.
- Sleep: Sleep mode minimizes power consumption by disabling all internal functional units, after which external system logic may disable the PPL and SUSCLK. Returning the PC755BM8 to the full-power state requires the enabling of the PPL and SYSCLK, followed by the assertion of an external asynchronous interrupt, a system management interrupt, a hard or soft reset, or a machine check input (MCP) signal after the time required to relock the PPL.

3.6.2 Power Dissipation

Table 3-5. Power Consumption
$V_{DD} = AV_{DD} = 2.0 \pm 0.1V$, $OV_{DD} = 3.3V \pm 5\%$ V_{DC}, GND = 0 V_{DC}, $0 \leq T_J < 105°C$

	Processor (CPU) Frequency/L2 Frequency		
	300/150 MHz	350/175 MHz	Unit
Full-on Mode			
Typical(1)(3)	4.1	4.6	W
Maximum(1)(2)	6.7	7.9	W
Doze Mode			
Maximum(1)(2)	2.5	2.8	W
Nap Mode			
Maximum(1)(2)	1700	1800	mW
Sleep Mode			
Maximum(1)(2)	1200	1300	mW
Sleep Mode-PLL and DLL Disabled			
Maximum(1)(2)	500	500	mW

Notes:
1. These values apply for all valid 60x bus and L2 bus ratios. The values do not include OV_{DD}; AV_{DD} and $L2AV_{DD}$ suppling power. OV_{DD} power is system dependent, but is typically < 10% of V_{DD} power. Worst case power consumption, for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at V_{DD} = 2.1V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at $V_{DD} = AV_{DD} = L2AV_{DD}$ = 2.0V, $OV_{DD} = L2OV_{DD}$ = 3.3V in a system, executing typical applications and benchmark sequences.

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4. Electrical Characteristics

4.1 Static Characteristics

Table 4-1. DC Electrical Specifications at Recommended Operating Conditions (see Table 3-3)

Characteristic	Nominal Bus Voltage(1)	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSLCK)(2)(3)	2.5	V_{IH}	1.6	(L2) OV_{DD} + 0.3	V
	3.3	V_{IH}	2	(L2) OV_{DD} + 0.3	V
Input low voltage (all inputs except SYSLCK)(2)	2.5	V_{IL}	–0.3	0.6	V
	3.3	V_{IL}	–0.3	0.8	V
SYSCLK input high voltage	2.5	KV_{IH}	1.8	OV_{DD} + 0.3	V
	3.3	KV_{IH}	2.4	OV_{DD} + 0.3	V
SYSCLK input low voltage	2.5	KV_{IL}	–0.3	0.4	V
	3.3	KV_{IL}	–0.3	0.4	V
Input leakage current, (2)(3) V_{IN} = $L2OV_{DD}$/OV_{DD}		I_{IN}	–	10	µA
Hi-Z (off-state) leakage current, (2)(3)(5) V_{IN} = $L2OV_{DD}$/OV_{DD}		I_{TSI}	–	10	µA
Output high voltage, I_{OH} = –6 mA	2.5	V_{OH}	1.7	–	V
	3.3	V_{OH}	2.4	–	V
Output low voltage, I_{OL} = 6 mA	2.5	V_{OL}	–	0.45	V
	3.3	V_{OL}	–	0.4	V
Capacitance, V_{IN} = 0V, f = 1 MHz (3)(4)		C_{IN}	–	5	pF

Notes:
1. Nominal voltages; See Table 3-3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).

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4.2 Dynamic Characteristics

After fabrication, parts are sorted by maximum processor core frequency as shown in Table 4-2 and tested for conformance to the AC specifications for that frequency. These specifications are for 275, 300, 333 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0-3] signals. Parts are sold by maximum processor core frequency.

4.2.1 Clock AC Specifications

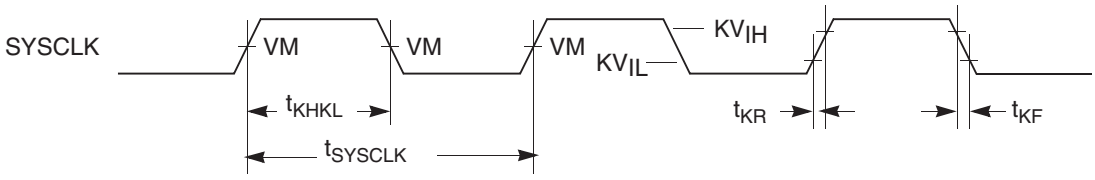
Table 4-2 provides the clock AC timing specifications as defined in Table 3-1.

Table 4-2. Clock AC Timing Specifications at Recommended Operating Conditions (See Table 3-3)

Characteristic	Symbol	Maximum Processor Core Frequency				Unit
		300 MHz		350 MHz		
		Min	Max	Min	Max	
Processor frequency(1)	f_{CORE}	200	300	200	350	MHz
VCO frequency(1)	f_{VCO}	400	600	400	700	MHz
SYSCLK frequency(1)	f_{SYSCLK}	25	100	25	100	MHz
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	ns
SYSCLK rise and fall time(2)	t_{KR} & t_{KF}	–	2	–	2	ns
	t_{KR} & t_{KF}	–	1	–	1	ns
SYSCLK duty cycle measured at $OV_{DD}/2$(3)	t_{KHKL}/t_{SYSCLK}	40	60	40	60	%
SYSCLK jitter(3)(4)		–	150	–	150	ps
Internal PLL relock time(3)(5)		–	100	–	100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description in Table 5-3," for valid PLL_CFG[0-3] settings
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1V/ns is equivalent to a 2 ns maximum rise/fall time measured at 0.4V and 2.4V or a rise/fall time of 1 ns measured at 0.4V to 1.4V.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter – short term and long term combined and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 4-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

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4.2.2 Processor Bus AC Specifications

Table 4-3 provides the processor bus AC timing specifications for the PC755BM8 as defined in Figure 4-2 and Figure 4-4.

Table 4-3. Processor Bus Mode Selection AC Timing Specifications(1) – At $V_{DD} = AV_{DD} = 2.0V$ 100 mV; $-55 \leq T_j \leq +125°C$, $OV_{DD} = 3.3V$ 165 mV and $OV_{DD} = 1.8V \pm 100$ mV and $OV_{DD} = 2.0V$ 100 mV

Parameter	Symbols(2)	All Speed Grades		Unit
		Min	Max	
Mode select input setup to $\overline{\text{HRESET}}$(3)(4)(5)(6)(7)	t_{MVRH}	8	–	t_{SYSCLk}
$\overline{\text{HRESET}}$ to mode select input hold(3)(4)(6)(7)(8)	t_{MXRH}	0	–	ns

Notes:
1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (see Figure 4-3). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going highs) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) – note the position of the reference and its state for inputs – and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX). For additional explanation of AC timing specifications in Freescale Power Architecture microprocessors, see the application note “Understanding AC Timing Specifications for Power Architecture Microprocessors.”
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4-3).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.
5. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in this table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0-3]
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

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Figure 4-2. Input/Output Timing Diagram

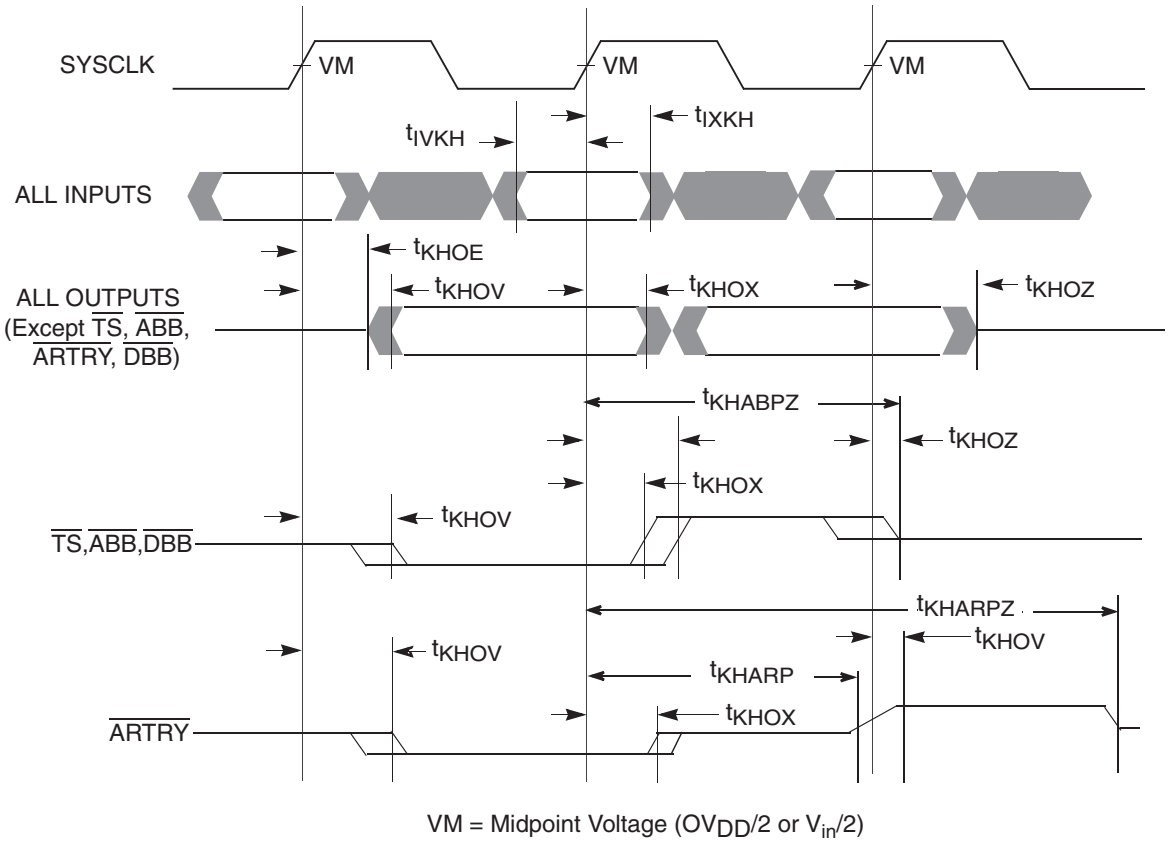


Figure 4-3. AC Test Load

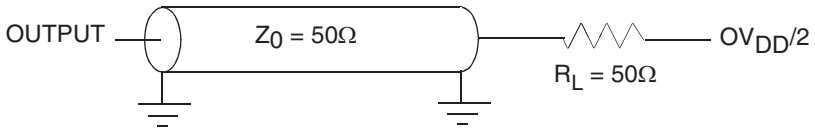
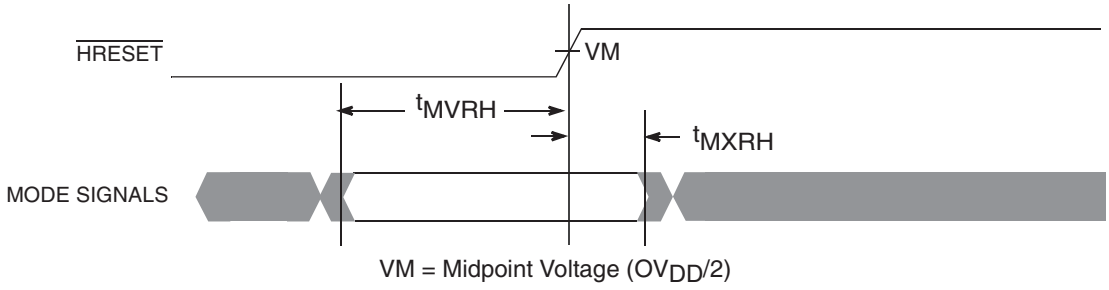


Figure 4-4. Mode Input Timing Diagram



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4.2.3 IEEE 1149.1 AC Timing Specifications

Table 4-4 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 4-5, Figure 4-6, Figure 4-7, and Figure 4-8.

Table 4-4. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

Parameter	Symbol	Min	Max	Unit
TCK Frequency of operation	f_{TCLK}	0	16	MHz
TCK Cycle time	f_{TCLK}	62.5	–	ns
TCK Clock pulse width measured at 1.4V	t_{JHJL}	31	–	ns
TCK Rise and fall times	t_{JR} & t_{JF}	0	2	ns
$\overline{TRST}$ Assert time[2]	t$\overline{TRST}$	25	–	ns
Input Setup Times:[3] Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 – –	ns
Input Hold Times:[3] Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 15 12	 – –	ns
Valid Times:[4] Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 – –	 4 4	ns
Output Hold Times:[4] Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 25 12	 – –	ns
TCK to output high impedance:[4][5] Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (See Figure 4-5). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 4-5. ALTERNATE AC Test Load for the JTAG Interface

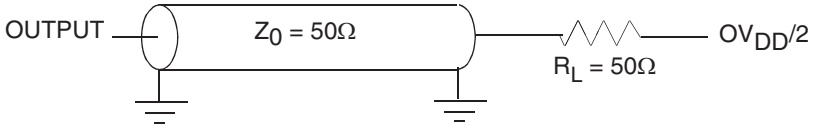

Figure 4-6. JTAG Clock Input Timing Diagram

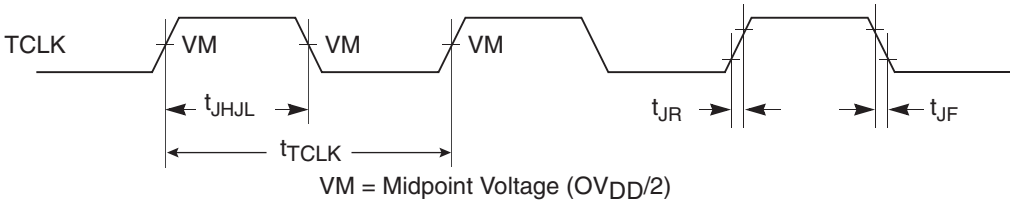

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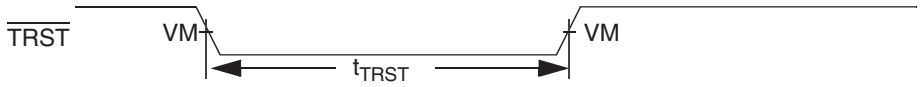
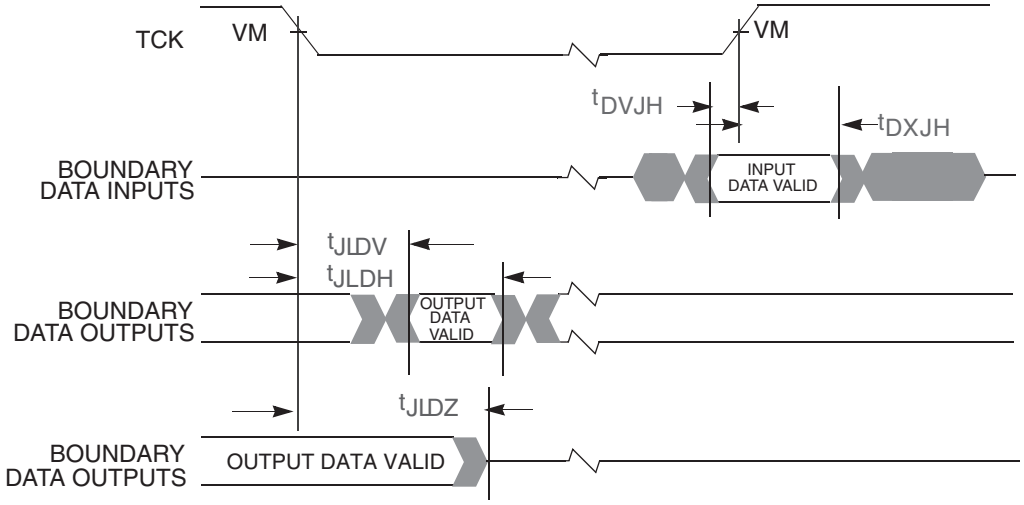
Figure 4-7. $\overline{\text{TRST}}$ Timing Diagram



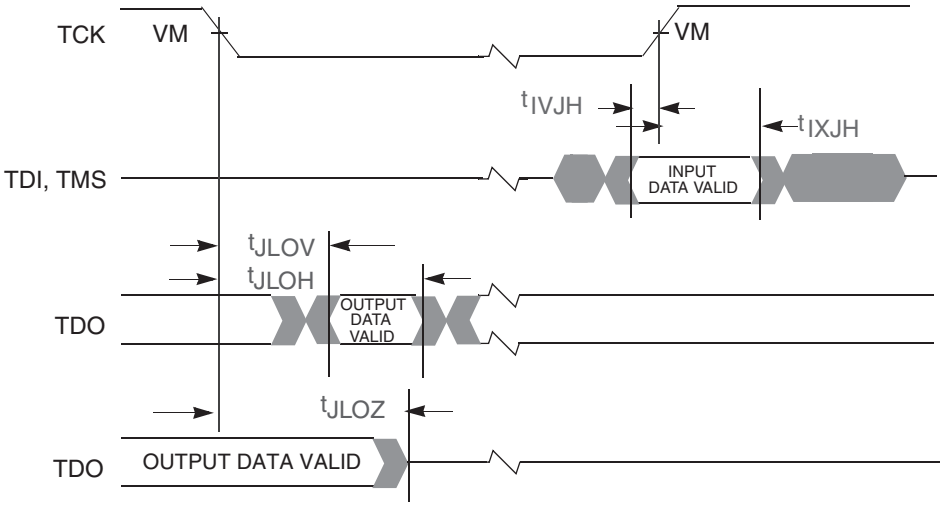
VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 4-8. Boundary-Scan Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 4-9. Test Access Port Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

5. Preparation for Delivery

5.1 Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

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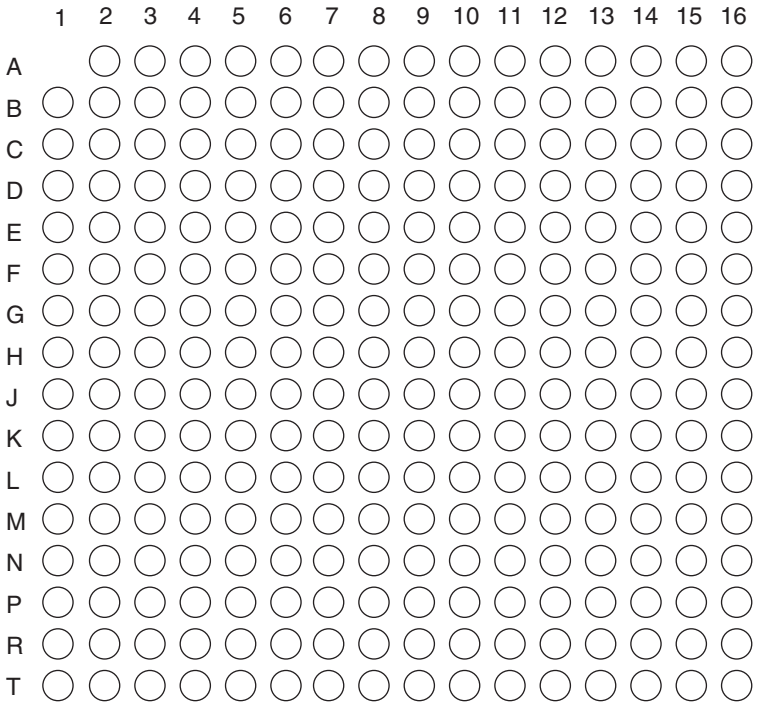
5.2 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces
- Ground test equipment, tools and operator
- Do not handle devices by the leads
- Store devices in conductive foam or carriers
- Avoid use of plastic, rubber, or silk in MOS areas
- Maintain relative humidity above 50 percent if practical

Figure 5-1. Pin Assignments

Ball assignments of the 255 CBGA package as viewed from the top surface



Side profile of the CBGA package to indicate the direction of the top surface view

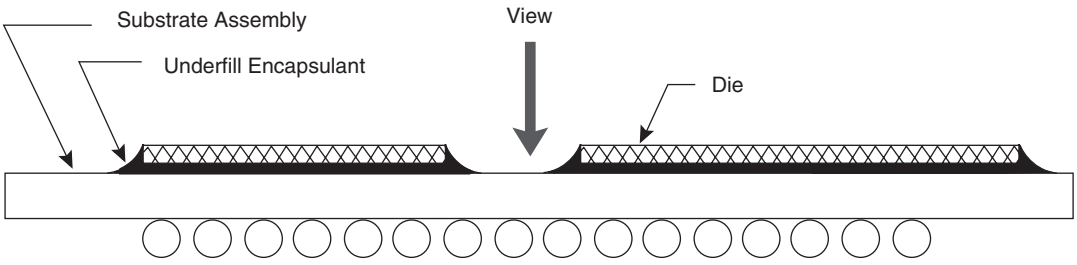


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Table 5-1. Package Pinout Listing

Signal Name	Pin Number	Active	I/O	2.0V[7]	3.3V[7]
A[0-31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	–	–
$\overline{\text{AACK}}$	L2	Low	Input	–	–
$\overline{\text{ABB}}$	K4	Low	I/O	–	–
AP[0-3]	C1, B4, B3, B2	High	I/O	–	–
$\overline{\text{ARTRY}}$	J4	Low	I/O	–	–
AV_{DD}	A10	–	–	2.0V	2.0V
$\overline{\text{BG}}$	L1	Low	Input	–	–
$\overline{\text{BR}}$	B6	Low	Output	–	–
BVSEL[4][5][6]	B1	High	Input	GND	3.3V
$\overline{\text{CI}}$	E1	Low	Output	–	–
$\overline{\text{CKSTP_IN}}$	D8	Low	Input	–	–
$\overline{\text{CKSTP_OUT}}$	A6	Low	Output	–	–
CLK_OUT	D7	–	Output	–	–
$\overline{\text{DBB}}$	J14	Low	I/O	–	–
$\overline{\text{DBG}}$	N1	Low	Input	–	–
$\overline{\text{DBDIS}}$	H15	Low	Input	–	–
$\overline{\text{DBWO}}$	G4	Low	Input	–	–
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	–	–
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	–	–
DP[0-7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	–	–
$\overline{\text{DRTRY}}$	G16	Low	Input	–	–
$\overline{\text{GBL}}$	F1	Low	I/O	–	–
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	–	–	GND	GND
HRESET	A7	Low	Input	–	–
$\overline{\text{INT}}$	B15	Low	Input	–	–
L1_TSTCLK[1]	D11	High	Input	–	–
L2_TSTCLK[1]	D12	High	Input	–	–
$L2AV_{DD}$	L11	–	–	2.0V	2.0V
$L2OV_{DD}$[8]	E10, E12, M12, G12, G14, K12, K14	–	–	2.0V	3.3V
L2VSEL[4][5][6][7]	B5	High	Input	[12]	3.3V
LSSD_MODE[1]	B10	Low	Input	–	–
$\overline{\text{MCP}}$	C13	Low	Input	–	–
NC (No-Connect)	C3, C6, D5, D6, H4, A4, A5, A2, A3	–	–	–	–
OV_{DD}[2]	C7, E5, G3, G5, K3, K5, P7, P10, E07, M05, M07, M10	–	–	–	–

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Table 5-1. Package Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O	2.0V[7]	3.3V[7]
PLL_CFG[0-3]	A8, B9, A9, D9	High	Input	–	–
$\overline{\text{QACK}}$	D3	Low	Input		
$\overline{\text{QREQ}}$	J3	Low	Output		
$\overline{\text{RSRV}}$	D1	Low	Output		
$\overline{\text{SMI}}$	A16	Low	Input		
$\overline{\text{SRESET}}$	B14	Low	Input	–	–
STCK[10]	B7	–	Input	–	–
STDI	C8	–	Input	–	–
STDO	J16	–	Output	–	–
STMS[11]	B8		Input		
SYSCLK	C9	–	Input	–	–
$\overline{\text{TA}}$	H14	Low	Input	–	–
TBEN	C2	High	Input	–	–
$\overline{\text{TBST}}$	A14	Low	I/O	–	–
TCK	C11	High	Input	–	–
TDI[6]	A11	High	Input	–	–
TDO	A12	High	Output	–	–
$\overline{\text{TEA}}$	H13	Low	Input	–	–
$\overline{\text{TLBISYNC}}$	C4	Low	Input	–	–
TMS[6]	B11	High	Input	–	–
$\overline{\text{TRST}}$[6]	C10	Low	Input	–	–
$\overline{\text{TS}}$	J13	Low	I/O	–	–
TSIZ[0-2]	A13, D10, B12	High	Output	–	–
TT[0-4]	B13, A15, B16, C14, C15	High	I/O	–	–
WT	D2	Low	Output	–	–
V_{DD}[2]	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9	–	–	2.0V	2.0V
VOLTDET[3]	F3	Low	Output	–	–

Notes:
1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core.
3. Internally tied to GND in the BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply pin.
4. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD} (Selects 3.3V Interface) or to GND (Selects 2.0V Interface).
5. Uses one of 15 existing no-connects in PC755BM8.
6. Internal pull up on die.
7. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR (0-16], L2DATA (0-63), L2DP{0-7] and L2SYNC-OUT) and the L2 control signals and the SSRAM power supplies; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$ respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see Recommended Operating Conditions.

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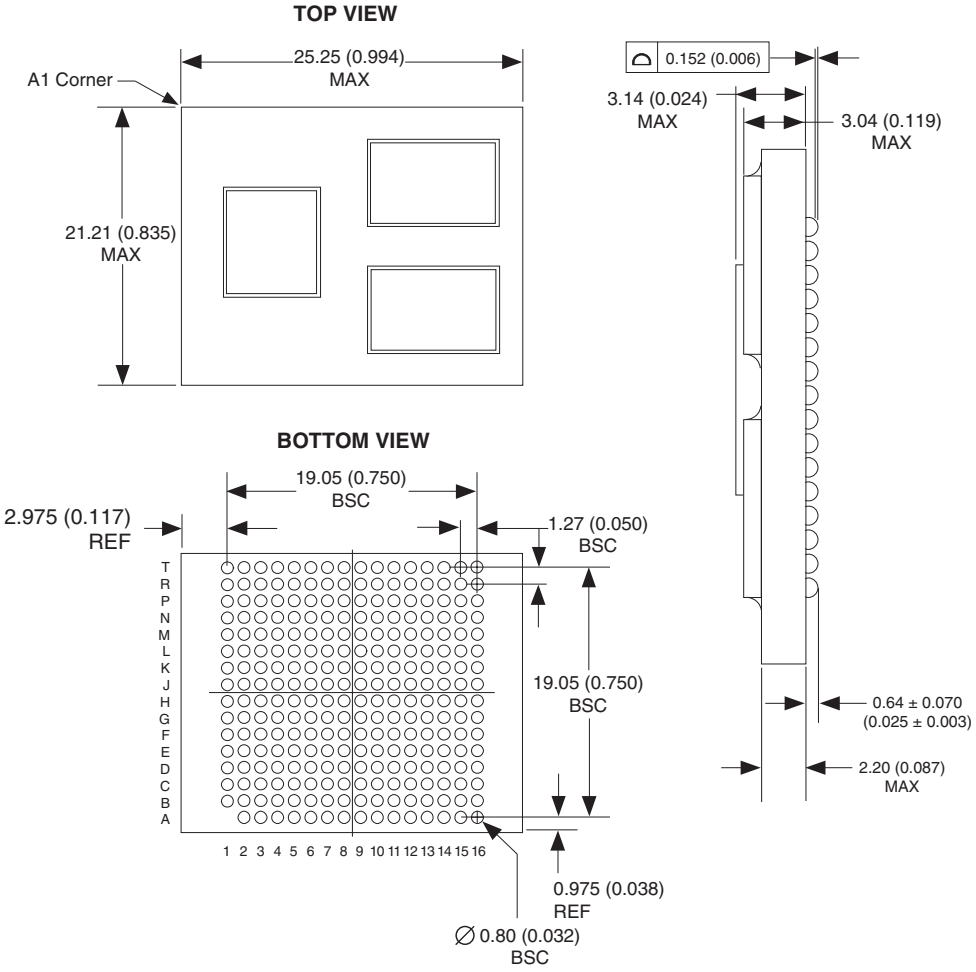
8. Uses one of 20 existing V_{DD} pins in PC755BM8, no board level design changes are necessary. For new designs of PC755BM8 refer to PLL power supply filtering.
9. $L2OV_{DD}$ for future designs that will require 2.OV L2 cache power supply – compatible with existing design using PC755BM8.
10. To disable SSRAM TAP controllers without interfering with the normal operation of the devices, STCK should be tied low (GND) to prevent clocking the devices.
11. STDI and STMS are internally pulled up and may be left unconnected. Upon power-up the SSRAM devices will come up in a reset state which will not interfere with the operation of the device.
12. Not supported on this version.

Table 5-2. Package Description

Package Outline	21 x 25 mm
Interconnects	255 (16 x 16 ball array less one)
Pitch	1.27 mm
Maximum Module Height	3.90 mm
Ball Diameter	0.8 mm

Figure 5-2. Package Dimensions 255 Ball Grid Array



Notes: 1. Dimensions in millimeters and paranthetically in inches.
2. A1 corner is designated with a ball missing the array.

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5.3 Clock Selection

The PC755BM8's PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC755BM8 is shown in Figure 6-2 for an example of frequencies.

Table 5-3. PC755BM8 Microprocessor PLL Configuration

PLL_CFG [0-3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	**Core-to VCO Multiplier**	**Bus 33 MHz**	**Bus 50 MHz**	**Bus 66 MHz**	**Bus 75 MHz**	**Bus 80 MHz**	**Bus 100 MHz**
0100	2x	2x	–	–	–	–	–	200 (400)
1000	3x	2x	–	–	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	–	–	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	–	200 (400)	266 (533)	300 (600)	320 (640)	–
0111	4.5x	2x	–	225 (450)	300 (600)	338 (675)	360 (720)	–
1011	5x	2x	–	250 (500)	333 (666)	–	–	–
1001	5.5x	2x	–	275 (550)	–	–	–	–
1101	6x	2x	200 (400)	300 (600)	–	–	–	–
0101	6.5x	2x	216 (433)	325 (650)	–	–	–	–
0010	7x	2x	233 (466)	350 (700)	–	–	–	–
0001	7.5x	2x	250 (500)	–	–	–	–	–
1100	8x	2x	266 (533)	–	–	–	–	–
0110	10x	2x	333 (666)	–	–	–	–	–
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC755BM8; See "Clock AC Specifications" on page 15. for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the PC755BM8 regardless of the SYSCLK input.

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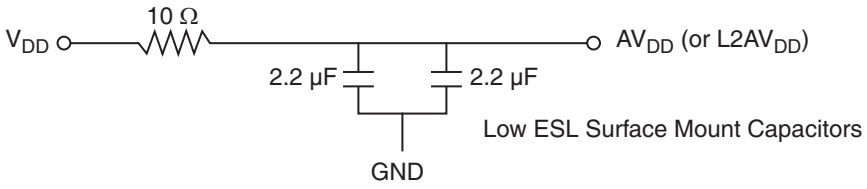
6. System Design Information

6.1 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the PC755BM8 to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 6-2 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route but is proportionately less critical.

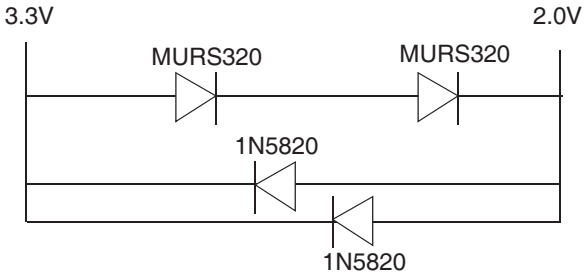
Figure 6-1. PLL Power Supply Filter Circuit



6.2 Power Supply Voltage Sequencing

The notes in Figure 6-3 contain cautions about the sequencing of the external bus voltages and core voltage of the PC755BM8 (when they are different). These cautions are necessary for the long term reliability of the part. If they are violated, the ESD (Electrostatic Discharge) protection diodes will be forward biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit of Figure 6-3 can be added to meet these requirements. The MUR420 Schottky diodes of Figure 6-3 control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

Figure 6-2. Example Voltage Sequencing Circuit



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6.2.1 Decoupling Recommendations

Due to the PC755BM8's dynamic power management feature, large address and data buses, and high operating frequencies, the PC755BM8 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC755BM8 system, and the PC755BM8 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the PC755BM8. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, (L2)OV_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 µF or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV vplanes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors – 100-330 µF (AVX TPS tantalum or Sanyo OSCON).

6.2.2 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the PC755BM8.

6.2.3 Output Buffer DC Impedance

The PC755BM8 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to (L2)OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is (L2)$OV_{DD}/2$ (See Figure 6-3).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals (L2)$OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals (L2)$OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices.

NO TAG describes the driver impedance measurement circuit described above.

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Figure 6-3. Driver Impedance Measurement Circuit

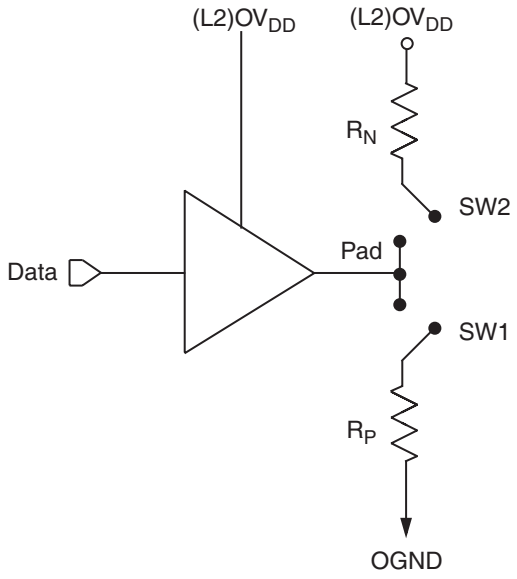

Table 6-1 summarizes the signal impedance results. The driver impedance values were characterized at 0° C, 65° C, and 105° C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 6-1. Impedance Characteristics – V_{DD} = 2.0V, OV_{DD} = 3.3V, T_c = 0 – 105° C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
RN	25-36	25-36	Z_0	W
RP	26-39	26-39	Z_0	W

6.2.4 Pull-up Resistor Requirements

The PC755BM8 requires pull-up resistors (1 kΩ – 5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the processor or other bus masters. These pins are $\overline{TS}$, $\overline{ABB}$, $\overline{AACK}$, $\overline{ARTRY}$, $\overline{DBB}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{TEA}$, and $\overline{DBDIS}$. $\overline{DRTRY}$ should also be connected to a pull-up resistor (1 kΩ – 5 kΩ) if it will be used by the system; otherwise, this signal should be connected to $\overline{HRESET}$ to select NO-DRTRY mode.

Three test pins also require pull-up resistors (100Ω – 1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation. In addition, $\overline{CKSTP_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ – 5 kΩ) if it is used by the system. During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the processor must continually monitor these signals for snooping, this float condition may cause additional power draw by the input receivers on the processor or by other receivers in the system. These signals can be pulled up through weak (10 kΩ) pull-up resistors by the system or may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw, but address bus pull-up resistors are not neccessary for proper device operation.

The snooped address and transfer attribute inputs are:

A[0:31], AP[0:3], TT[0:4], $\overline{TBST}$, and $\overline{GBL}$.

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The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If 32-bit data bus mode is selected, the input receivers of the unused data and parity bits will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

6.3 JTAG Configuration Signals

Figure 6-4. Suggested $\overline{\text{TRST}}$ Connection

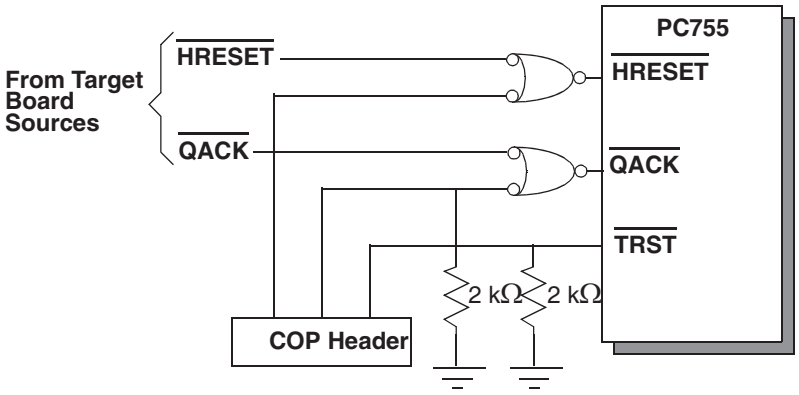

Figure 6-5. COP Connector Diagram

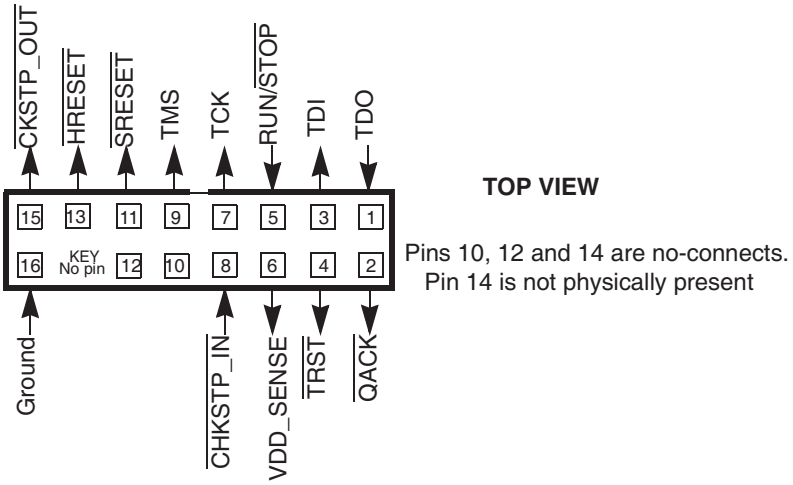

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Table 6-2. COP Pin Definitions

Pins	Signal	Connection	Special Notes
1	TDO	TDO	
2	$\overline{\text{QACK}}$	$\overline{\text{QACK}}$	A_{DD} 2K pull-down to ground. Must be merged with on-board $\overline{\text{QACK}}$, if any.
3	TDI	TDI	
4	$\overline{\text{TRST}}$	$\overline{\text{TRST}}$	A_{DD} 2K pull-down to ground. Must be merged with on-board $\overline{\text{QACK}}$, if any. See Figure 6-4.
5	RUN/$\overline{\text{STOP}}$	No connect	Used on 604e; leave no-connect for all other processors.
6	VDD_SENSE	VDD	A_{DD} 2K pull-up to OV_{DD} (for short circuit limiting protection only).
7	TCK	TCK	
8	$\overline{\text{CKSTP_IN}}$	$\overline{\text{CKSTP_IN}}$	Optional. A_{DD} 10K pull-up to OVDD. Used on several emulator products. Useful for checkstopping the processor from a logic analyzer of other external trigger.
9	TMS	TMS	
10	N/A		
11	$\overline{\text{SRESET}}$	$\overline{\text{SRESET}}$	Merge with on-board SRESET, if any.
12	N/A		
13	$\overline{\text{HRESET}}$	$\overline{\text{HRESET}}$	Merge with on-board $\overline{\text{HRESET}}$
14	N/A		Key location; pin should be removed.
15	$\overline{\text{CKSTP_OUT}}$	$\overline{\text{CKSTP_OUT}}$	A_{DD} 10K pull-up to OVDD.
16	Ground	Digital Ground	

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all Power Architecture implementations. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Since the JTAG interface is also used for accessing the common on-chip processor (COP) function of Power Architecture processors, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ isn't practical.

The common on-chip processor (COP) function of Power Architecture processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 6-4 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while insuring that the target can drive $\overline{\text{HRESET}}$ as well. The pull-down resistor on $\overline{\text{TRST}}$ ensures that the JTAG scan chain is initialized during power-on if a JTAG interface cable is not attached; if it is, it is responsible for driving $\overline{\text{TRST}}$ when needed.

The COP header shown in Figure 6-5 adds many benefits – breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

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7. System design information

The COP interface has a standard header for connection to the target system, based on the 0.025” square-post 0.100” centered header assembly (often called a “Berg” header). The connector typically has pin 14 removed as a connector key, as shown in Figure 6-5.

8. Definitions

8.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnity e2v for any damages resulting from such improper use or sale.

9. Document Revision History

Table 9-1 provides a revision history for this hardware specification.

Table 9-1. Document Revision History

Rev. No	Date	Substantive Change(s)
D	06/2007	Name change from Atmel to e2v Ordering information update
C	09/2005	Ordering information changed Motorola changed to Freescale

10. Ordering Information

xx	755B	M	8	y	G	nnn	L	E
Product Code (1)	Part Identifier	Multichip Package	L2 cache density	Temperature Range T_J (1)	Package (1)	Core frequency	Bus divider (to be confirmed)	Revision Level (1)
PC(X) (2)	755BM8		8 Mbits: 128K x 72 SSRAM	M: -55˚C, +125˚C V: -40˚C, +110˚C	G: CBGA	300: 300 MHz/150 L2 cache 350: 350 MHz/175 MHz L2 cache	L: Any valid PLL configuration	E: Rev. 2.8

Notes:
1. For availability of the different versions, contact your local e2v sales office.
2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

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